Serial No.: 10/056,657

: October 19, 2001 Filed Page

ley Docket No.: 10559-524001 Intel Docket No.: P12428

**REMARKS** 

Claims 1 to 20 are pending in the application, of which claims 1 and 11 are the independent claims. Applicants hereby affirm the telephone election of claims 1 to 20. Nonelected claims 21 to 25 have been cancelled. Favorable reconsideration and further examination are respectfully requested.

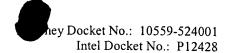
Initially, the Examiner disapproved the drawings filed May 7, 2002 for lack of support in the original specification for two multifunctional pumps connected in cascade. FIG. 1 has been modified to correct the title of reference 70 from "multifunctional pump" to "regulation switch." In FIG. 3, the bracket for reference 10 was extended to include reference 20. Applicants submit herewith proposed drawing corrections, which includes the foregoing changes. Approval of these drawing corrections is respectfully requested.

Turning to the specification rejections, claims 11 to 13 and 15 to 20 were rejected under 35 U.S.C. §112, first paragraph. Specifically, comparator 40 was alleged by the Examiner to be critical to the practice of the invention. Without conceding the propriety of the rejection, or the criticality of the comparator to the claims, and solely to advance prosecution, Applicants have amended claims 1 and 11 to reference a comparator. Withdrawal of the rejection is requested.

Claims 1 to 20 were rejected under 35 U.S.C. §112, first paragraph, for allegedly containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In particular, the Examiner alleges that the specification fails to disclose how to make and use the circuit of FIG. 2, because the Examiner further alleges that

Serial No.: 10/056,657 : October 19, 2001 Filed

Page



there is no such element as an array. One example of an array is noted in the specification: "Each array is a circuit array that includes switches, capacitors, and transistors configured similar to any standard voltage pump configuration" (see page 4 line 3-5). Applicants submit that it is well known in the art how to construct a voltage pump, as evidence by the disclosures of voltage pumps cited by the Examiner. Accordingly, Applicants respectfully request that an "array" would be understandable to those skilled in the art armed with the disclosure of the subject application and, therefore, request withdrawal of the rejection...

Claims 2, 5, 7 to 10, 12, 15 and 17 to 20 were rejected under 35 U.S.C. §112, second paragraph, for allegedly failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

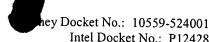
Regarding claim 2, the Examiner alleges that there is no support in the specification for "the square waveform." Applicants have indicated in the specification that "system 10 provides ... a square wave signal" (see page 3 line 9). Specifically, the "multifunctional pump 20 slews from a read level voltage ... to a program level voltage ... and back down to a verify voltage" (see page 3 lines 2-4). In view of this disclosure, Applicant respectfully requests that the rejection be withdrawn.

Regarding claim 5, the Examiner alleges that the term "array" is not understood. In addition, the Examiner alleges claim 5 is not supported by the specification because arrays in parallel are not disclosed. In response, claim 5 has been amended to recite that "each array is a circuit array configured to form a voltage pump." Claim 5 has also been amended to include clock drivers corresponding to each array and that each clock driver and array are in parallel.

Serial No.: 10/056,657

Filed : October 19, 2001

Page



Intel Docket No.: P12428

Regarding claim 7, the Examiner alleges that a multifunctional pump cannot have a standby mode or a read mode. Applicants have amended claim 7 to recite only a standby mode.

Regarding claim 8, the Examiner alleges a read pump is not understood in the art.

Applicants have amended claim 8 to recite placing the multifunctional pump in a read mode.

Regarding claim 9, the Examiner alleges a standby pump is not understood in the art. Applicants have amended claim 9 to recite placing the multifunctional pump in a program mode.

Regarding claim 10, the Examiner alleges a program/erase pump is not understood in the art. Applicants have amended claim 10 to recite placing the multifunctional pump in an erase mode.

In view of the foregoing amendments and remarks, Applicants respectfully request withdrawal of the §112, second paragraph, rejections.

The claims stand rejected over U.S. Patent No. 6,339,547 (Roohparvar) and U.S. Patent No. 6,246,280 (Morishita). As shown above, Applicants have amended the claims to define the invention with greater clarity. In view of these clarifications, reconsideration and withdrawal of the art rejections are respectfully requested.

Claim 1 is directed to a method of providing multiple voltage outputs. The method includes receiving an input signal from a multifunctional pump configured to provide more than two voltages, sending a first output signal based on the input signal using a first switch, sending the input signal to a transistor, and sending a second output signal received from the transistor via a second switch. The method also includes comparing a reference voltage and a feedback voltage using a first comparator to provide a comparator result using the first comparator that is coupled to a gate of the transistor to control the transistor based on the comparator result.

Serial No.: 10/056,657 Filed : October 19, 2001

Page : 11 ney Docket No.: 10559-524001 Intel Docket No.: P12428

Roohparvar is not understood to disclose or to suggest the foregoing features of claim 1. In particular, Roohparvar is not understood to disclose or to suggest at least "sending a second output signal received from the transistor via a second switch" and "comparing a reference voltage and a feedback voltage using a first comparator to provide a comparator result, the first comparator being coupled to a gate of the transistor to control the transistor based on the comparator result."

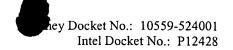
More specifically, Roohparvar does not show a gate of a transistor coupled to a comparator. Rather, Roohparavar shows transistor gates coupled to a voltage, Vcc (see, e.g., Fig. 4, transistors 142, 144, 146). Moreover, Roohparvar is not understood to disclose or to suggest at least "receiving an input signal from a multifunctional pump configured to provide more than two voltages." Rather, Roohparvar shows receiving only a constant program voltage (i.e., 12 volts) or zero volts (see, e.g., column 7, lines 25 et seq.).

The deficiencies in Roohparvar are not cured by combining Roohparvar and Morishita. In particular, Morishita does not receive "an input signal from a multifunctional pump configured to provide more than two voltages." FIG. 9, which the Examiner cites in Morishita. shows a voltage regulator that provides either  $V_{nn}$  or  $V_{bb}$ , i.e., only two voltages. The claim calls for receipt from a multifunctional pump providing more than two voltages.

Moreover, Morishita is not understood to disclose or to suggest at least "sending a second output signal received from the transistor via a second switch" and "comparing a reference voltage and a feedback voltage using a first comparator to provide a comparator result, the first comparator being coupled to a gate of the transistor to control the transistor based on the comparator result." To meet these limitations, the Examiner suggested replacing the Voltage

Serial No.: 10/056,657 Filed: October 19, 2001

Page: 12



Regulator 320 with the feedback amplifier of FIG. 9. However, in this combination, there would be no second output signal received from the transistor via a second switch because the second switch precedes the transistor (which is in the voltage regulator, i.e., transistor 520).

Accordingly, contrary to what was said in the Office Action, the resulting hypothetical combination of Roohparvar and Morishita would not meet the limitations of the claims.

For the foregoing reasons, claim 1 should be allowed.

Claim 11 is an apparatus claim that roughly corresponds to amended claim 1. Claim 11 and its dependent claims are believed to be allowable for at least the same reasons noted above with respect to claim 1 and its dependent claims.

In view of the foregoing amendments and remarks, the entire application is believed to be in condition for allowance and such action is respectfully requested at the Examiner's earliest convenience.

Applicants undersigned attorney can be reached by telephone at the number shown below. All correspondence should continue to be directed to Scott Harris in our San Diego office.

Enclosed is a check for \$110 for a One-Month Extension of Time. No other fee is believed to be due for this Amendment; however, if any other fees are due, please apply such fees to Deposit Account No. 06-1050 referencing Attorney Docket 10559-524001.

Serial No.: 10/056,657 Filed: October 19, 2001

Page : 13

hey Docket No.: 10559-524001 Intel Docket No.: P12428

Respectfully submitted,

Date: 4ebricy 25, 2603

ATTORNEYS FOR INTEL Fish & Richardson P.C. 225 Franklin Street Boston, Massachusetts 02110-2804

Telephone: (617) 542-5070 Facsimile: (617) 542-8906

20547548.doc

Paul A. Pysher Reg. No. 40,780

Serial No.: 10/056,657
Filed: October 19, 2001

Page : 14

hey Docket No.: 10559-524001 Intel Docket No.: P12428

## VERSION WITH MARKINGS TO SHOW CHANGES MADE

## IN THE SPECIFICATION:

Paragraph beginning at page 2, line 21 has been amended as follows:

--For multifunctional pump system 10 to function properly, the system provides multiple outputs and multiple voltage levels to satisfy requirements of an external circuit (not shown). For example, when multifunctional pump 20 is in the program mode, multifunctional pump 20 slews from a read level voltage (e.g., 5 volts (V)) to a program level voltage (e.g., 7 V) and back down to a verify level voltage (e.g., 5V). [At the same time,] Another output provides a constant voltage (e.g., 5 V) [is required to supply a Flash Algorithm Code Storage (FACS), for example, to allow a proper sensing voltage level at the wordlines of the FACS array, thus keeping the software running correctly]. [Thus, since system] System 10 provides both a square wave signal and a constant voltage [, one output from multifunction pump 20 does not satisfy both requirements].--

Paragraph beginning at page 3, line 20 has been amended as follows:

--Referring to FIG. 2, multifunctional pump 20 includes a comparator 12, an oscillator 14, clock drivers (e.g., first clock driver 16a, second clock driver 16b, third clock driver 16c, fourth clock driver 16d, and fifth clock driver 16e), arrays (e.g., first array 18a, second array 18b, third array 18c, fourth array 18d, and fifth array 18e), and a feedback network 22. Each array is a circuit array that includes switches, capacitors, and transistors configured similar to any standard voltage pump configuration. Comparator 12 receives input, IN<sub>1</sub>, and compares IN<sub>1</sub> to a

Serial No.: 10/056,657

: October 19, 2001

Filed Page

: 15

Docket No.: 10559-524001

Intel Docket No.: P12428

feedback signal F<sub>1</sub>. If feedback signal F<sub>1</sub> is less than input signal IN<sub>1</sub>, then comparator 12 turns-

on oscillator 14. Oscillator 14 then supplies an oscillating signal to each of the clock drivers

16a-e. When activated, each of the clock drivers 16a-e supply a signal to a corresponding array

18a-e. The output from each array 18a-e are connected to a node 24 so that an output signal, IN<sub>2</sub>,

is measured from node 24. In this embodiment, oscillator 14 is a four phase clock.--

Paragraph beginning at page 6, line 4 has been amended as follows:

-- Regulation switch 70 as shown in Fig. 3 includes a comparator 40, a first transistor 42

(e.g., p-channel metal oxide semiconductor), a first switch 44, and a second switch 46.

Comparator 40 receives a feedback voltage, F<sub>2</sub>, and compares it to a reference voltage, R<sub>1</sub>, when

enabled by a fourth enable signal, E<sub>4</sub>. Feedback voltage F<sub>2</sub>, connects a transistor source 45 to

comparator 40. If F<sub>2</sub> is less than R<sub>1</sub>, comparator 40 regulates a gate 43 of first transistor 42.

[First transistor 42 acts as a series regulation switch. Thus, transistor 42 is turned-on when the

voltage of transistor gate 43 drops below a threshold voltage, V<sub>T</sub>, of transistor 42. However, as

the voltage increases from comparator 40 to transistor gate 43, the first transistor 42 gradually

turns-off so that the transistor is off when the voltage at transistor gate 43 is greater than IN<sub>2</sub>-

 $V_T$ . For example, when  $IN_2 = 4.8 \text{ V}$  and  $V_T = 0.7 \text{ V}$ , transistor 42 turns off at gate voltages

greater than 4.1 volts.] --

IN THE CLAIMS:

Claim 4, 14 and 21 to 25 have been cancelled.

Claim 1, 3, 5 to 13 and 15 to 20 have been amended as follows:

Serial No. : 10/056,657

Filed: October 19, 2001

Page : 16

ley Docket No.: 10559-524001 Intel Docket No.: P12428

--1. (Amended) A method of providing multiple voltage outputs, comprising:

receiving an input signal from a multifunctional pump configured to provide more than
two voltages;

sending a first output signal based on the input signal using a first switch; [and] sending the input signal to a transistor;

sending a second output signal [based on the input signal] <u>received from the transistor</u> [using] <u>via</u> a second switch [and a transistor]; and

comparing a reference voltage and a feedback voltage using a first comparator to provide a comparator result, the first comparator being coupled to a gate of the transistor to control the transistor based on the comparator result.

- 3. (Amended) The method of claim 2, wherein the first output signal has a [maximum] voltage of 7 volts and a [minimum] voltage of 5 volts and the second output signal is 5 volts.
- 5. (Amended) The method of claim 1, wherein the multifunctional pump is a circuit comprises [comprising]:
  - a first array receiving input from a first clock driver;
- a second array <u>receiving input from a second clock driver</u>, the second clock driver and the <u>second array being</u> in parallel to the first array <u>and the first clock driver</u>;
- a third array receiving input from a third clock driver, the third clock driver and the third array being in parallel to the second array and the second clock driver;

Serial No.: 10/056,657 Filed : October 19, 2001

Page : 17 ney Docket No.: 10559-524001

Intel Docket No.: P12428

a fourth array receiving input from a fourth clock driver, the fourth clock driver and the fourth array being in parallel to the third array and the third clock driver; and

a fifth array receiving input from a fifth clock driver, the fifth clock driver and the fifth array being in parallel to the fourth array and the fourth clock driver; wherein each array is a circuit array configured to form a voltage pump.

6. (Amended) The method of claim 5, wherein the multifunctional pump further comprises [comprising]:

an oscillator providing a clock signal to each of the clock drivers [arrays]; and a second comparator providing input to the oscillator, the second comparator comparing the output from the arrays with a predetermined voltage.

7. (Amended) The method of claim 6, [wherein] <u>further comprising</u>:

placing the multifunctional pump [is] in a standby mode when the first clock driver [array] is enabled by a first signal[, wherein the multifunctional pump is in read mode when the second array is enabled by a second signal and the first array is on, and wherein the pump is in a program/erase mode when the third array, the fourth array, and the fifth array are enabled by a third signal and the first array and the second array are on].

8. (Amended) The method of claim [1] 6, [wherein] further comprising: placing the multifunctional pump is in a read mode when the second clock driver is enabled by a second signal and the first array is on [a read pump].

Serial No.: 10/056,657 Filed: October 19, 2001

Page : 18

્રં

ney Docket No.: 10559-524001 Intel Docket No.: P12428

9. (Amended) The method of claim [7] 6, [wherein] further comprising:

placing the multifunctional pump [is] in a program mode when the third clock driver, the fourth clock driver, and the fifth clock driver are enabled by a third signal and the first array and the second array are on [a standby mode pump].

10. (Amended) The method of claim [8] 6, [wherein] further comprising:

placing the multifunctional pump [is] in an erase mode when the third clock driver, the fourth clock driver, and the fifth clock driver are enabled by a third signal and the first array and the second array are on [a program/erase pump].

- 11. (Once Amended) An apparatus for providing multiple voltages, comprising:
- a multifunctional pump configured to provide more than two voltages;
- a first switch receiving input from the multifunctional pump and providing a first output signal;
  - a transistor receiving input from the multifunctional pump;
- a first comparator coupled to a gate of the transistor to control the transistor based on a comparator result, the first comparator comparing a reference voltage and a feedback voltage to provide the comparator result; and
  - a second switch, coupled to the transistor, providing a second output signal.

Serial No.: 10/056,657 Filed

: October 19, 2001

Page : 19

ney Docket No.: 10559-524001 Intel Docket No.: P12428

13. (Amended) The apparatus of claim 12, wherein the first output signal has a [maximum] voltage of 7 volts and a [minimum] voltage of 5 volts and the second output signal is 5 volts.

15. (Once Amended) The apparatus of claim 11, wherein the multifunctional pump comprises:

a first array receiving input from a first clock driver:

a second array receiving input from a second clock driver, the second clock driver and the second array being in parallel to the first array and the first clock driver;

a third array receiving input from a third clock driver, the third clock driver and the third array being in parallel to the second array and the second clock driver:

a fourth array receiving input from a fourth clock driver, the fourth clock driver and the fourth array being in parallel to the third array and the third clock driver; and

a fifth array receiving input from a fifth clock driver, the fifth clock driver and the fifth array being in parallel to the fourth array and the fourth clock driver:

wherein each array is a circuit array configured to form a voltage pump.

16. (Amended) The apparatus of claim 15, wherein the multifunctional pump further comprises [comprising]:

an oscillator providing a clock signal to each of the clock drivers [arrays]; and a second comparator providing input to the oscillator, the second comparator comparing the output from the arrays with a predetermined voltage.

Serial No.: 10/056,657 Filed: October 19, 2001

Page : 20

ney Docket No.: 10559-524001 Intel Docket No.: P12428

17. (Amended) The apparatus of claim 16, wherein the multifunctional pump is in standby mode when the first clock driver [array] is enabled by a first signal[, wherein the multifunctional pump is in read mode when the second array is enabled by a second signal and the first array is on, and wherein the pump is in a program/erase mode when the third array, the fourth array, and the fifth array are enabled by a third signal and the first array and the second array are on].

- 18. (Amended) The apparatus of claim [11] 16, wherein the multifunctional pump is in read mode when the second clock driver is enabled by a second signal and the first array is on [a read pump].
- 19. (Amended) The apparatus of claim [18] 16, wherein the multifunctional pump is in a program mode when the third clock driver, the fourth clock driver, and the fifth clock driver are enabled by a third signal and the first array and the second array are on [a standby mode pump].
- 20. (Amended) The apparatus of claim [19] 16, wherein the multifunctional pump is in an erase mode when the third clock driver, the fourth clock driver, and the fifth clock driver are enabled by a third signal and the first array and the second array are on [a program/erase pump].--